IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	: 10/510,567	Confirmation No.	: 9020
First Named Inventor	: Hirohisa MIYAZAWA		
Filed	: October 8, 2004		
TC/A.U.	: 2841		
Examiner	: TUAN T. DINH		
Docket No.	: 029267.55488US		
Customer No.	: 23911		
Title	: Circuit Board Device for Information Apparatus, Multilayered Module Board and Navigation System		

REPLY BRIEF

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

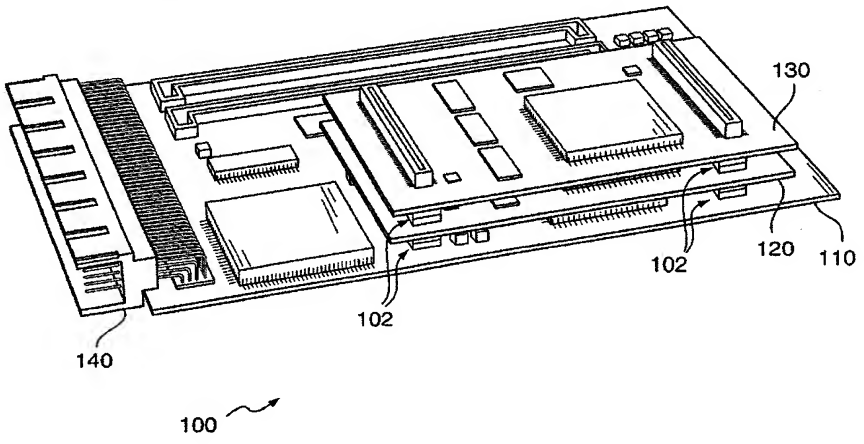
In complete response to the Examiner's Answer mailed on July 25, 2008, Appellant hereby submits a Reply Brief pursuant to 37 C.F.R. § 41.41.

As will be discussed in detail below, the Examiner's Answer does not demonstrate that there is an express or inherent disclosure in the applied prior art of all of the features of Appellant's claim 1, the combination of prior art does not disclose or suggest all of the features of claims 7 and 8, and the Patent Office's position with respect to the rejection of claim 1 is unclear.

1. Khosrowpour Does Not Expressly or Inherently Disclose a Multilayer Module Board Including at Least a CPU and a Memory

As previously discussed, the Patent Office relies upon Figure 1 of Khosrowpour (reproduced below) as anticipating the board with a CPU and memory of Appellant's claim 1. Specifically, the Patent Office asserts that the unlabeled "bigger chip" discloses the claimed CPU and the unlabeled "three chip reside near to the square chip" corresponds to the claimed memory.

FIG. 1



In response to Appellant's arguments that there is no express or inherent support in Khosrowpour for the Patent Office's interpretation of Figure 1, the Patent Office now cites a new reference to support the Patent Office's position on inherency. This new reference, U.S. Patent No. 5,615,211 to Santore et al. ("Santore"), does not support the Patent Office's position that *all daughterboards must* include a CPU and memory. Instead, while Santore discloses that the

particular telecommunication circuit boards 30 disclosed by Santore include a microprocessor 124 and buffers 114 and 118, there is nothing in Santore that *all daughterboards must* include a processor and memory.

As previously discussed, inherency is not established by probabilities or possibilities, but instead requires that the extrinsic evidence makes "clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill."[1] Accordingly, the "mere fact that a certain thing may result from a given set of circumstances is not sufficient."[2] Thus, the mere fact that Santore discloses that a *particular* telecommunication circuit board includes a microprocessor and buffers does not mean that *all daughterboards must* include a processor and memory.

Moreover, the particular telecommunication circuit boards of Santore are disclosed as being commercially available from General DataComm, Inc., whereas the Khosrowpour is assigned to Adaptec, Inc. Thus, even if it were assumed that Santore disclosed that all circuit boards from General DataComm, Inc. included processors and memories, which Santore does not, this would not mean that *all daughterboards from Adaptec, Inc. must* include a processor and memory.

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[1] M.P.E.P. § 2112, citing *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).
[2] *Id.*

Because Khosrowpour does not expressly or inherently disclose a daughterboard with a processor and memory, and the newly cited Santore patent does not disclose that *all daughterboards must* include a processor and memory, the Patent Office has not provided a prior art reference that discloses all of the elements of Appellant's claim 1.

2. Khosrowpour Does Not Expressly or Inherently Disclose the Type of Claimed Multilayer Module Board

As previously discussed, Khosrowpour does not expressly or inherently disclose a multilayer module board mounted on a base board, and is one of a low-end module board, a high-speed module board or an advanced function module board. In response to this argument the Examiner's Answer cites column 4, lines 9-21 of Khosrowpour as disclosing that "there are many types of the daughterboard (120, 130) are accepted by motherboard (110), and the low end module board, the high speed module board, **or** the advance function module board is very broad that covers every types of the board."[3]

Column 4, lines 9-21 (reproduced below for convenience), however, does not expressly or inherently disclose that the daughterboard is one of a low-end module board, a high-speed module board or an advanced function module board.

> FIG. 1 illustrates an embodiment of a stacked circuit board assembly 100 according to the present invention. A motherboard 110 includes a connector 140, e.g., a backplane connector.

[3] Pages 7-8, emphasis in the original.

> Daughterboards 120, 130 are stacked on the motherboard 110 in a so-called "mezzanine" arrangement. The motherboard 110 and the daughterboards 120, 130 are interconnected by a plurality 102 of connectors. Those skilled in the art will appreciate that the motherboard 110 and the daughterboards 120, 130 may comprise boards employing using through-hole or surface-mounted devices on single or multi-layer printed circuit boards (PCBs), as well as more exotic board structures constructed using, for example, thick-film or co-fired ceramic technologies.

Furthermore, Appellant's claim 1 specifically recites one of three different types of boards, and therefore the Patent Office's position that the claim "covers every types of the board" ignores this express claim element.

Because Khosrowpour does not expressly or inherently disclose the type of claimed multilayer module board, Khosrowpour does not anticipate claim 1 for this additional reason.

3. The Rejection of Claims 7-9 for Obviousness in View of the Combination of Khosrowpour and Yasuho is Improper

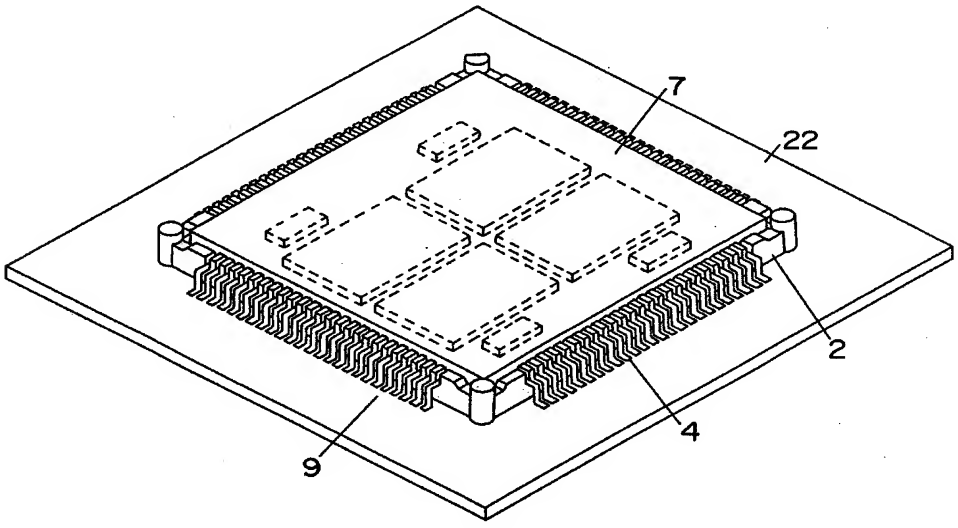
In response to Appellant's repeated requests for a citation to Yasuho of a disclosure of the elements of claims 7-9, the Patent Office finally provides such a citation. This newly provided citation, however, does not disclose or suggest the elements of claims 7-9.

Appellant's claim 7 and independent claim 9 both recite four connector terminals that "each include a narrow, elongated base portion *constituted of resin*

and a plurality of pins affixed to the base portion."[4] Claim 8 recites a similar element.

The Patent Office now makes clear that the rejection is based upon an interpretation of terminals 4 of Yasuho (illustrated in Figure 21 reproduced below).

FIG. 21



Yasuho, however, does not disclose or suggest that these terminals "include a narrow, elongated base portion *constituted of resin*."[5] Instead, these terminals are likely constituted of some type of metal in order to transfer electrical signals. Thus, the newly cited portion of Yasuho does not disclose or suggest the four connector terminals recited in Appellant's claims 7-9, and the combination of Khosrowpour and Yasuho does not render these claims obvious.

[4] Emphasis added.
[5] Emphasis added.

4. **The Patent Office's Position on the Disclosure of Khosrowpour is Unclear**

In response to Appellant's arguments in the Reply filed July 30, 2007, that Khosrowpour does not disclose the particular type of multilayer board recited in claim 1, the Office Action mailed on October 18, 2007, cited U.S. Patent No. 5,025,306 to Johnson et al ("Johnson") as extrinsic evidence that the daughterboard of Khosrowpour is inherently a multilayer board. Based on the Examiner's Answer, it now appears that the Patent Office asserts that Khosrowpour expressly discloses this claim feature. In order to provide a clear record for the Board's review of this application the Patent Office should clarify how it is interpreting Khosrowpour.

5. Conclusion

Because the Khosrowpour does not expressly or inherently disclose all of the elements of Appellant's claim 1, and the combination of Khosrowpour and Yasuho does not disclose or suggest all of the elements of Appellant's claims 7-9, the rejection of these claims is improper and should be reversed.

The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, to Deposit Account No. 05/1323, Docket No.: 029267.55488US.

Respectfully submitted,

September 24, 2008

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